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ADVANCED COMMUNICATION ESM SYSTEM (ACES) DESIGN CONSIDERATIONS (U)

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DEFENCE RESEARCH ESTABLISHMENT OTTAWA
TECHNICAL NOTE 92-2

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ADVANCED COMMUNICATION ESM SYSTEM (ACES) DESIGN CONSIDERATIONS (U)

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Electronic Warfare Division

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ABSTRACT

This note outlines the proposed design and development of the Advanced Communication ESM System (ACES) testbed in the Communication Electronic Warfare (CEW) Section at DREO. The purpose of this testbed is to develop a high probability of intercept (POI) ESM system for use against various conventional and exotic HF and VHF communications signals. This work is being carried out in support of the army (D-Sigs-EM2) under Task 041XG. The ACES testbed will use wideband digital receivers and advanced digital signal processors to provide high POI, real-time signal detection and identification, high resolution DF, data fusion, analysis, and C^3I functions. The aim is to produce a complete ESM system suitable for field trials in a real signal environment by March 1994.

RESUME

Cette note technique contient un aperçu de la conception et de la mise en oeuvre du banc d'essai du Système Avancé de Communication pour MSE (SACM) par la Section des communications pour la guerre électronique de CRDO. Le banc d'essai est conçu pour la mise au point d'un système de MSE à grande Probabilité d'Interception (PI) qui sera utilisé contre divers signaux de communication HF and VHF, conventionnels ou exotiques. Ce travail est effectué pour l'armée (DTTM2) dans le cadre de la demande 041XG. Le banc d'essai du SACM utilisera des récepteurs numériques à grande bande passante et des unités de traitement numériques avancées pour produire une PI élevée, la détection et l'identification des signaux en temps réel, du pointage à haute résolution, de la fusion des données, de l'analyse et des fonctions C^3I. L'objectif est de produire, d'ici mars 1994, un système complet de MSE pour des essais sur le terrain dans un environnement de signaux réels.

EXECUTIVE SUMMARY

This note describes the proposed design and development of the Advanced Communications Electronic Warfare Support Measures (ESM) System (ACES) testbed in the Communications Electronic Warfare (CEW) Section at DREO. The purpose of the testbed is to provide a high probability of intercept (POI) ESM system for use against various conventional and exotic HF and VHF communications signals. This work is being carried out in support of the army (D-Sigs-EM2) under Task 041XG.

The variety, sophistication, and abundance of communications equipment encountered in any modern conflict poses many challenges to communications electronic warfare operations. Even low intensity conflicts could present hundreds of different signals that must be collected, processed, and analyzed by a communications ESM system. These signals reside, for the most part, within the HF, VHF, and UHF frequency bands. The signals of interest (SOI) include those which are of the conventional analog type (signals with FM, AM, SSB, etc. modulations), conventional digital (BPSK, QPSK, FSK, etc. modulations), and exotic signals including those of short duration and those which are frequency agile.

To be effective on the modern battlefield, a communications ESM system requires a level of sophistication beyond present conventional systems. Such a system would consist of many closely integrated sub-systems, each performing a specialized function and feeding data to a central command, control, and analysis system. Sub-system functions include signal detection with 100% POI, multi-channel intercept for all SOI, high resolution direction-finding (DF), modulation recognition, signal finger-printing, data fusion and analysis, and C^{3}I. Many of the performance requirements for these sub-systems are beyond the current state-of-the-art. The problems of communicating and correlating the data from each sub-system pose many challenges in system integration. As such the ACES testbed will not only provide a platform for on-going development of new ESM techniques but will also be an exercise in system development.

The ACES testbed will consist of existing testbeds in CEW, as well as off-the-shelf, state-of-the-art, and experimental components. Existing testbeds include the Radio Direction Finding (DF) testbed, Adaptive Signal Processing Testbed (ASPT), and the Data Fusion And Correlation Techniques Testbed (DFACTT) [1]. Off-the-shelf components include SUN4/370™ [1] workstations,

[1] SUN is a trademark of Sun Microsystems.

TMS320C30™ [2] DSPs, and WJ-8617B receivers. State-of-the-art and experimental technologies include Regal™ [3] [3] FFT processors, iWarp™ [4] array processors [4], wideband high dynamic range digital RF receivers, and neural networks. The main focus of the ACES project will be on algorithm and software development, and component integration. An iterative approach will be taken in developing ACES. This will produce an evolving experimental system that will address each function individually while also supporting overall system integration and functionality.

ACES will be developed in three phases starting April 1991. Phase 1 will consist of a single channel system using a low dynamic range receiver and SUN-based TMS320C30 DSPs. It will provide a basis for conducting experiments in interference excision, modulation recognition and spectral estimation. It will be completed by March 1992.

Phase 2 will also be a single channel system and will consist of two parts. Phase 2A will introduce a high dynamic range wideband digital receiver front-end, a real-time FFT processor for spectral estimation, and a PC-based TMS320C30 DSP for signal detection. This phase will produce a system capable of limited real-time operation by August 1992. Phase 2B will augment the PC-based C30 with the SUN-based iWarp array processors. The iWarps will serve as a platform for studying advanced signal processing algorithms and neural networks. This phase will produce a high POI system capable of real-time signal detection, finger-printing, and identification by March 1993.

Two separate testbeds will be developed concurrently during this period, the DF testbed and the DFACTT. Phase 3 will integrate these testbeds into ACES and incorporate multiple wideband digital receivers to provide a high resolution DF capability and the data fusion, analysis, and C^3I system. This phase will produce a complete ESM system suitable for field trials in a real signal environment by March 1994.

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[2] The TMS320C30 is a trademark of Texas Instruments Incorporated.

[3] Regal is a trademark of Austek Incorporated, Adelaide, Australia.

[4] iWarp is a trademark of Intel Corporation.

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1.0 INTRODUCTION

1.1 Aim

The aim of this note is to outline a system design for a proposed testbed called the Advanced Communication ESM System (ACES). This testbed will be developed at the Defence Research Establishment Ottawa with industrial support. The development will entail the integration of a combination of off-the-shelf and state-of-the-art hardware components geared towards forming an environment to conduct research in a host of communications ESM-related functions. Several of these functions include signal interception, detection, modulation recognition, signal isolation, bearing location, and data fusion and correlation.

1.2 Background

Communications ESM is primarily concerned with intercepting, detecting, and locating radio communication signals. There are a number of ancillary functions which such systems must perform too, as stated in Section 1.1.

There are many types of signals which are of interest to a Communications-EW (Comms-EW) operator. These signals reside, for the most part, within the HF, VHF, and UHF frequency bands. The signals of interest include those which are of the conventional analog (signals with FM, AM, SSB, etc. modulations), conventional digital (BPSK, QPSK, FSK, etc. modulations), and exotic signal (short duration and frequency agile) types.

The signal environment in the HF, VHF and UHF bands is potentially quite dense. For example, if one assumes 5 KHz spacing between channels in the HF (3 - 30 MHz) band, there are 5400 channels to monitor. Compounding the problem are the varying bandwidths, modulations and amplitudes of the signals, rendering detection and identification of signals of interest very difficult. Conventional analog processing methods are inadequate to process all these channels quickly. However, modern digital hardware and processing techniques are at a state of maturity to provide the capabilities and performance levels needed to meet the above challenges.

With this in mind, the ACES testbed will be an exercise in the integration of new analog and digital processing technologies into an experimental ESM testbed. In addition, it will provide a facility for the development and study of digital signal processing algorithms for spectral estimation, energy detection, modulation recognition, conventional and high resolution DF, signal finger-printing, sensor data fusion and C^3I.

1.3 Scope

Section 2 of this paper describes the nature of the problems involved in modern communications Electronic Warfare. Section 3 outlines the specifications for an advanced ESM system. Section 4 describes the system components available for developing the ACES testbed. Section 5 proposes an approach to integrating these components into a functional ESM system and details its development. Section 6 presents some concluding remarks on the challenges facing this project.

2.0 DESCRIPTION OF PROBLEM

Communications ESM is mainly used to support the Electronic Warfare (EW) activities of the land forces. The tasks that make up Comms-ESM operations include intercepting, processing and identifying a variety of signals within the HF, VHF and UHF frequency bands; determining the direction and location of the sources of the intercepted signals; and correlation and analysis of this information. These tasks are not trivial, given the plethora of signals to be processed and their increasing sophistication.

As alluded to in Section 1.2, the challenges confronting a modern-day ESM system are many. A more comprehensive list is presented here. For example:

a. the signals of interest can be located anywhere within the HF and VHF/UHF bands (3 MHz - 3 GHz)

b. these bands contain thousands of signals that are not of interest

c. various modulation schemes, both analog and digital, are used

d. signal bandwidths can range from 100 Hz to several MHz

e. signal durations can range from milliseconds to several minutes

f. signal dynamic ranges can be as much as 90 dB

g. the signal environment changes dynamically

h. the signals must be identifiable by their characteristics

i. all signal parameters must be combined for identification and analysis, and

j. signals of interest must be sorted out from the signals not of interest for further processing.

These problems impose stringent requirements on a Comms ESM system. The most crucial are: large spurious-free dynamic range ($\approx$90 dB); fast scan rate; fine frequency resolution ($\approx$100Hz); fine time resolution ($\approx$1ms); multiple and concurrent interception/detection/DF of a wide variety of signals; and real-time sorting, correlation, and data analysis.

Previous approaches to these problems have been only partially successful in meeting these requirements. For example, compressive IF receivers have the required scanning rates but have insufficient dynamic range. On the other hand, scanning receivers have excellent dynamic range and resolution, but are too slow. In addition, current processing methods are slow and rely on post-processing of stored raw sensor data, resulting in data that may be stale. New systems require more flexibility to meet the broad range of requirements.

To address the above problems a. to j., a highly integrated, highly-digital signal and analysis processing approach is required. The following section describes the specifications of such a system.

3.0 ACES SYSTEM SPECIFICATIONS

The ACES project is concerned with developing an ESM system with a very high POI and high accuracy DF for signals of interest. The proposed system will have to be flexible and expandable in terms of processing performance and architecture. This will allow the system to adapt to the requirements of the algorithms developed instead of limiting their implementation.

The overall ACES system will consist of four components: the receivers; the signal intercept/detection sub-system; the DF sub-system; and the data fusion/analysis/C^3I sub-system. A brief description of the specifications for each component follows.

3.1 Receiver Specifications

The front-end sensors for this system will consist of radio-frequency receivers. The basic requirements for the radio receivers are: wide instantaneous bandwidth; multiple signal intercept; and high dynamic range. Trade-offs between each of these desired characteristics must be made based on the current and expected level of available RF receiver technology.

Conventional narrowband scanning receivers do not provide the speed required to detect or intercept short duration or frequency agile signals with a high degree of probability. Micro-scan receivers, on the other hand, are also limited in dynamic range, although they have an exceptionally high POI capability.

It appears that ultra-linear wide-band receivers with highly linear analog-to-digital conversion units and high speed FFT processors are the most promising. It is important to underline the importance of the analog-to-digital converters. They are critical components since they tend to exhibit non-linearities at high sampling rates for increasing numbers of bits, which in turn affects the dynamic range specification. A list of desired receiver specifications is shown in Table 3.1.

TABLE 3.1: DESIRED RECEIVER SPECIFICATIONS

1. RF Frequency Range:	3 - 1000 MHz
2. Instantaneous Analysis Bandwidth:	> 2 MHz
3. Spurious Free Dynamic Range:	> 90 dB
4. Digital IF output:	Sample rate depending on bandwidth. Word length depending on dynamic range.

Other desired features of a receiver include computer controlled tuning, electronic switching between multiple antennas, and phase referencing. One final consideration is the data rate and the number of bits/sample at the output of the receiver. These parameters will have a major impact on the processors selected for the systems following the receivers, i.e., the interception, detection, and DF systems. For example, if the data rate is too high, certain processors would not be able to keep up, leading to a reduction in detection probability.

3.2 Signal Detection System Specifications

The signal detection system will consist of two parts, i.e., the spectral estimation processor and the energy detection and alarm processor.

3.2.1 Spectral Processor

Since the signal from the receivers will be digital, both spectral estimation and energy detection will be performed with digital processors. The data rate and wordlength of the data will govern processor selection and performance. The desired spectral processor specifications are shown in Table 3.2.

TABLE 3.2: DESIRED SPECTRAL ESTIMATION PROCESSOR SPECIFICATIONS

1.	Algorithm:	Fast Fourier Transform (FFT)
2.	Input Sample Rate: examples:	> twice Receiver BW receiver BW = 2 MHz, sample rate > 4Ms/s receiver BW = 10 MHz,sample rate > 20 Ms/s
3.	Transform Size: examples:	2 * receiver BW / frequency resolution[5] BW: 2 MHz, Res: 1 kHz, Size = 4k BW: 10 MHz, Res: 1 kHz, Size = 16k BW: 2 MHz, Res: 100 Hz, Size = 64k BW: 10 MHz, Res: 100 Hz, Size = 256k
4.	Transform Time for continuous operation: examples:	Frequency Resolution / (2 * receiver BW) BW: 2 MHz, Res: 1 kHz, rate > 4 Ms/s Transform Time: **4k FFT in < 1 ms** BW: 10 MHz, Res: 1 kHz, rate > 20 Ms/s Transform Time: **16k FFT in < 1 ms** BW: 2 MHz, Res: 100 Hz, rate: > 4 Ms/s Transform Time: **64k FFT in < 10 ms** BW: 10 MHz, Res: 100 Hz, rate > 20 Ms/s Transform Time: **256k FFT in < 10 ms**
5.	Event Resolution:	Twice the Transform times shown above
6.	Word length:	Dynamic Range = $10*\log_2(2^{2/B}/4N)$ db [2], B = Number of bits in a word N = FFT Transform size
	examples:	Dynamic range: 90dB 1k FFT requires: 21 bits 4k FFT requires: 22 bits 16k FFT requires: 23 bits 64k FFT requires: 24 bits 256k FFT requires: 25 bits

[5] Frequency resolution is defined as the reciprocal of the observation time, i.e., N/f_s, where N is the FFT size and f_s is the sampling rate.

As can be seen, there are trade-offs between bandwidth, frequency resolution, and event resolution. Based on the current state of digital processing technology, there is an upper limit on the processing power that can be applied to these problems. Also, in order to have a re-configurable system that will meet a host of experimental and operational requirements, the spectral processor must be programmable. All of these factors must be weighed in selecting a processing system.

3.2.2 Signal Detection System Specifications

The energy/signal detection processor operates on the output of the spectral processor. The spectral processor will provide an array of frequency bins containing amplitude and phase information. The energy detection processor must perform array averaging, thresholding, and correlation operations on this data. In order to achieve 100% POI and probability of detection (POD), these operations must be performed in real time, implying that all detection processing be completed in the same time span required to produce each spectral array vector. The energy detection processor must also provide detection alarms and low-level signal descriptors (bandwidth, centre frequency, and time) to an overall system controller for signal isolation, DF and modulation recognition processors.

3.3 Intercept/DF System Specifications

The goal is to develop an N-channel DF system capable of intercepting and DF'ing a variety of signals within, initially, the HF/VHF frequency bands. Digital processing techniques will be used to effect this function.

Several options will be possible to carry out the DF'ing function, depending on the hardware configuration. If N = 2, the antenna system/combining network results in two channels, one being the reference, the other a signal whose phase will determine the DF. If N = 3, then one can have, say, an L-shaped antenna configuration, producing an interferometric DF system. For N = 8 elements, experiments in high resolution DF can be conducted.

Wideband and/or narrowband receivers will be used. DF accuracy will depend on the hardware and algorithms used and is one of main areas of research in this project. The DF will be tasked from the high level control system or the signal detection system. In some cases, DF will be integrated with intercept processing. In other cases it will be separate. The configuration used will depend on the particular experiment to be conducted.

When using wideband receivers, the narrowband SOI must first be filtered out of the wideband data stream and mixed to near baseband to reduce the sample rate. This may require special digital hardware for each digital intercept channel.

Integration of the intercept and DF functions with the rest of the system will present many difficulties. A multi-channel system will require many data paths and complex control functions. The wide variety of message and data types as well as various data rates and formats will complicate system integration. This is one of the serious challenges facing the ACES project.

3.4 Data Fusion and C^3I System Specifications

Multi-sensor fusion is the process of correlating information about the same situation from different sensors to produce a more accurate estimate or model of the situation than can be obtained from the individual sensors. Command, Control, Communications and Intelligence (C^3I) are the four main functions required to effectively integrate system components.

An ESM system must gather and interpret electronic sensor data to provide useful intelligence information for other systems, such as those concerned with either ECM or SIGINT operations.

C^3I can be combined into one high-level system component having several important functions:

a. reception of all sensor data including intercept messages, signal descriptors, DF readings, signal alarms

b. fusion and correlation of sensor data

c. provision of the man/machine interface to the system

d. storage of all information and maintenance of the database

e. control and steerage of all sensors

f. situation analysis and report generation

g. dissemination of information (SIGINT/COMINT) to other units.

Since the ESM system is expected to operate continuously, the fusion system must be able to process all sensor data as fast as it is gathered or it will lose valuable information, thus reducing the system's effectiveness.

The sensors will produce multiple concurrent intercept and DF messages as well as spectral information and energy alarms for processing. The nature of the processing required may include the use of advanced methods such as expert systems and neural networks. Some level of human analysis will also be needed, requiring a powerful user-interface. The resulting information must then be stored and disseminated. The system must also be closely integrated with the sensors to provide active feedback throughout the system.

4.0 AVAILABLE SYSTEM COMPONENTS

The specifications presented in Section 3 are very ambitious and stress the limits of current technology in many areas. Some of the technologies meet these requirements, others have only recently emerged. Furthermore, most of these technologies are provided by a limited number of foreign manufacturers.

As an example, the specifications for the spectral processor are still considered to be at or beyond the current state-of-the-art in digital processing. However, the ACES testbed will be incorporating some of this new or untried technology. This will pose certain risks to the project, but it is felt that the specifications can be met by using this new technology.

Other important factors, such as cost and development time, must also be considered in defining a feasible system architecture. The approaches proposed here are all based on the utilization of several systems or technologies which are either under development, or currently existing in the Communications EW section (CEW) of DREO. Integration of these systems with new technology, where required, will reduce the overall level of risk and the cost of developing a system capable of meeting most, if not all, of the outlined specifications in a reasonable period of time.

There are several sub-systems either being developed or existing in CEW which will provide components for developing or testing the ACES testbed. These include:

a. DF Antenna
b. DF Testbed
c. DAR 4000 Digitizer
d. Adaptive Signal Processing Testbed
e. SUN 4/370 Development System
f. Complex Waveform Simulator
g. HP9000/345 Computer System
h. Communication Radio Testbed
i. Data Fusion and Correlation Techniques Testbed (DFACTT)

The following is a short description of each sub-system and their possible contribution to the ACES project.

4.1 DF Antenna

This is a circular phased DF array for the 30 - 90 MHz band. The antenna produces two signal channels such that the phase relationship between the channels represents the signal's bearing.

4.2 DF Testbed

This testbed is being developed by McMaster University. It will be capable of detailed measurements of multipath propagation phenomena for research into high resolution DF techniques.

4.3 DAR 4000 Digitizer

The DAR 4000 digitizes a wideband analog signal centered at an IF of 21.375 MHz using a bandpass sampling approach. The sampling rate is 12.5 Msamples/sec. The system then splits the data into I and Q components and provides these as the output at a rate of 6.25 Msamples/sec.

4.4 Adaptive Signal Processing Testbed

This testbed consists of a SUN 3/470 VME-based workstation and multiple TMS320C30 DSP boards designed to operate in parallel. It will be capable of performing most of the processing required for the specified intercept/DF operations. It will also be capable of carrying out spectral estimation and detailed signal analysis on much lower data rates than those entering the proposed spectral estimator discussed earlier.

4.5 SUN 4/370 Development System

This workstation will be a development platform for the spectral processors (i.e., the Austek boards) and the signal detection processors (i.e., the iWarp boards), both of which will be discussed later.

4.6 Complex Waveform Simulator

The complex waveform simulator can simulate a wide range of digital communication signals in the frequency bands 2 - 30 MHz, 50 - 90 MHz, 225 - 400 MHz, and 600 - 950 MHz. Its primary purpose is to produce spread spectrum signals (Direct Sequence (DS), Frequency Hopping (FH), or Time Hopping (TH)). The data modulation for the spread spectrum portion is either BPSK or QPSK. The system can also generate hybrids of the spread spectrum signals.

4.7 HP9000/345 Computer System

The HP9000/345 is a computer system with HPIB interface and post processing software package for the HP8568B Spectrum Analyzer. This system is capable of producing 3-D waterfall displays of the HP8568B output. It will prove useful for analyzing low resolution, low dynamic range signals.

4.8 Communication Radio Testbed

The radio testbed provides a range of analog signals for input into a receiver. It can produce modulated signals which are either AM, FM, or SSB. The modulating signal in this case is baseband audio. The IF can be anywhere between 2 - 1000 MHz. It also has the capability of producing FSK signals in the frequency range 2 - 500 MHz.

4.9 Data Fusion and Correlation Techniques Testbed (DFACTT)

This testbed consists of hardware and software for communication ESM sensor data fusion and analysis. It is of modular design and uses object-oriented software to allow for easy development and expansion. Phase 3 of the ACES system development specifies integration with an ESM sensor system to be supplied by DREO. The DFACT testbed can provide most of the C^3I and analysis functions required by the ACES testbed.

5.0 PROPOSED SYSTEM DEVELOPMENT

ACES will be developed in three phases, the first two using a single receiver and the third employing multiple receivers. Phase 1 will concentrate on developing experience in digital signal processing. It will also include simulations and non-real time processing of wideband signals. Phase 2 will involve more advanced signal processing including real-time spectral analysis, signal detection, mixing, demodulation, and signal extraction. Phase 3 will expand the system to include direction finding capabilities and advanced processing techniques. A schedule depicting the planned development of ACES is shown in Figure 5.1

5.1 Phase 1

Phase 1 will concentrate on the fundamentals of digital signal processing. This will include algorithm development and implementation on actual DSP chips. The main platform for this development will be the Adaptive Signal Processing Testbed (ASPT) which was briefly described in Section 4. The focus of this phase will be to:

a. interface to a low dynamic range digital receiver (WJ-8617 and DAR 4000)

b. study TMS320C30 processors using the ASPT

c. develop C30 software to calculate FFT's and experiment with complex digital mixing, Finite Impulse Response (FIR) filtering and adaptive filtering algorithms

d. develop and test modulation recognition algorithms, and

e. develop user interfaces and control software.

A block diagram of this phase of the ACES testbed is shown in Figure 5.2. Software for the TMS320C30 processors will be developed on the SUN host computer. High level signal processing design software for the host will be developed during Phase 1. These tools will be instrumental in software development for ACES during all phases of the project. There is some element of risk associated with the C30 processor boards since they are custom hardware currently under development. Phase 1 is expected to be completed by July 1992.

5.2 Phase 2

Phase 2 will be a single channel system consisting of two parts, i.e., 2A and 2B. This phase will greatly increase the scope, functionality, and complexity of the ACES testbed. Phase 2A will introduce a high dynamic range wideband digital receiver front-end, a real-time FFT processor for spectral estimation, and a

PC-based TMS320C30 DSP for signal detection. Narrowband analog receivers will be used to isolate SOI's. This phase will produce a system capable of limited real-time operation by October 1992.

Phase 2B will involve replacing the PC-based C30 with the SUN-based iWarp array processors. The iWarps will serve as a platform for studying advanced signal processing algorithms. Digital drop receivers will replace the analog drop receivers used in Phase 2A. To account for processing delays through the Austeks and iWarps, digital delay lines will be included, therefore ensuring no loss of data. This phase will produce a high POI system capable of real-time signal detection, finger-printing, and identification by April 1993.

The following is a short description of each of the various components to be used during Phase 2.

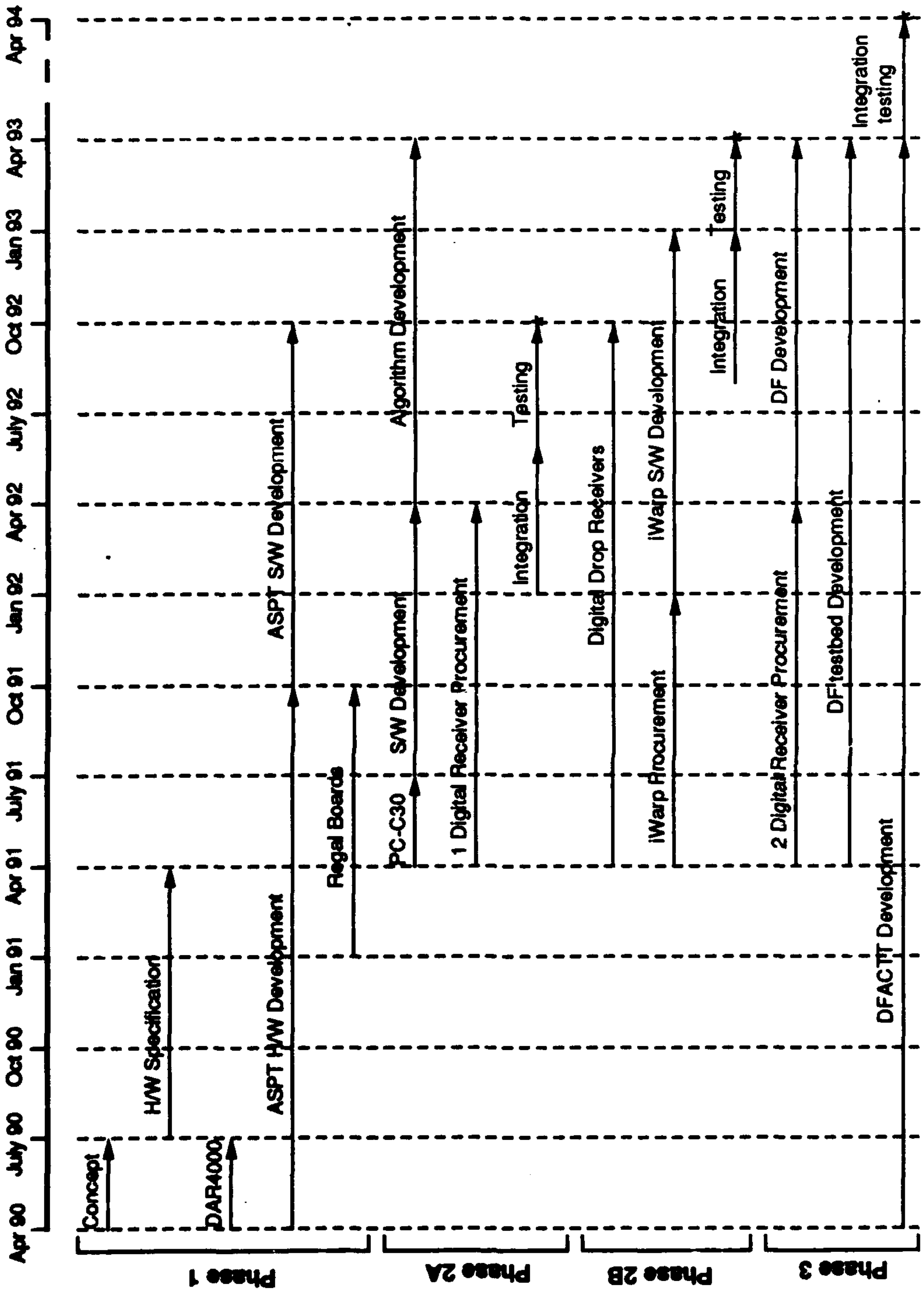

FIGURE 5.1: ACES DEVELOPMENT SCHEDULE

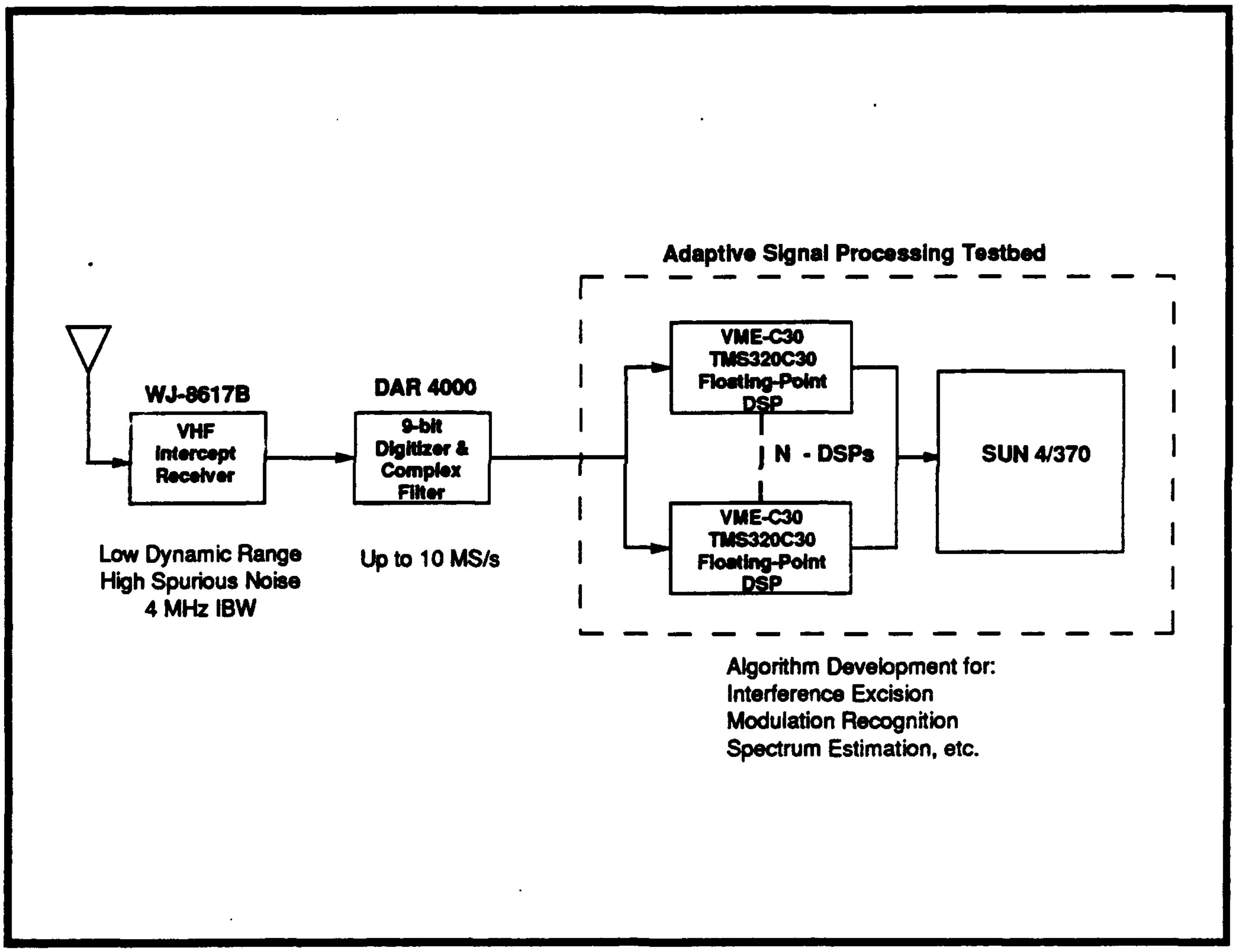

FIGURE 5.2: ACES PHASE 1

5.2.1 **Wideband Digital Tuner**

The plan is to procure three RF Digitizers from Steinbrecher Inc., Model DT14088. The frequency range of this model is 1.5 - 88 MHz, with an instantaneous signal analysis bandwidth of 2 MHz, and a spurious free dynamic range of 85 dB. The data rate is 5 MSamples/second with 14 bits/sample.

Only one Steinbrecher receiver will be used in Phase 2. It will act as the primary sensor for signal intercept and will provide the data source for the FFT processor. It will also act as a data source for multiple narrowband digital drop receivers which will be used for SOI isolation for the DF function, modulation recognition, and signal fingerprinting.

5.2.2 **FFT Processor**

ACES will use an FFT board developed by Austek Microsystems of Australia. The board is referred to as the Regal Dual-FFT Module A98113. It can carry out FFT's on blocks ranging in size from 512 - 64K points on a continuous data rate of 6 million complex samples/second. It supports integer word sizes of 16, 20 and 24 bits. It can perform a 65536 point complex FFT every 10.9 milliseconds at a continuous rate. For example, for a 2 MHz instantaneous bandwidth, this processor could resolve signals less than 100 Hz apart and differing in amplitude by 85 dB with an event time of about 11 milliseconds.

The role of these boards in the system will be to conduct spectral estimation. These boards will be interfaced to the C30 processor in a 486 PC (Phase 2A) and iWarp processors (Phase 2B). The Austek processor is proven technology, so the level of risk is expected to be low.

5.2.3 **PC-Based TMS320C30 System**

This C30 system is different from the ASPT VME-C30 system described earlier. Its purpose is to provide an initial analysis tool for the Austek boards. The software to analyze and display spectral data from the Austek boards has already been developed at DSTO in Australia. Therefore, the start-up time for this aspect of the work will be short. The plan is to have the algorithms transferred to the iWarp system. The PC-based C30 system will also be used to simulate target signals which will be processed by the rest of system.

The Phase 2A system using this hardware is shown in Figure 5.3. The Austek FFT processor will be situated in a SUN4/370 computer already procured. The ASPT C30 boards will be used in the SUN4/370 being delivered as part of the ASPT. Signal detection will be performed by a TMS320C30 card in a 486 PC with 19" colour monitor.

5.2.4 **iWarp Array**

The iWarp is a parallel processor produced by Intel and is designed for signal and image processing [4]. Each iWarp processor, or cell, has a peak performance of 20 MIPS and 20 MFLOPS. An iWarp array is linearly scalable from 4 cells (80 MFLOPS) to 1024 cells (20 GFLOPS). For budgetary reasons, ACES will be using an 8 cell array providing a computational capability of 160 MFLOP's and 160 MIP's.

The iWarp processors are designed to perform linear algebra functions. This implies matrix operations, convolutions, FFT's, QR-decomposition, filtering operations, and other linear algegra operations at very high data rates.

The iWarp boards will reside in the SUN 4/370 VME computer system, and will be used to process the FFT data vectors from the Regal processors discussed above, performing such operations as spectral smoothing and signal detection. Being a new product, the level of risk could be moderately high.

5.2.5 **Channel Recovery Processors**

The channel recovery processors are equivalent to narrowband drop receivers. In the ACES system, their role will be to recover (or isolate) narrowband signals with bandwidths less than 100 kHz from the wideband 2 MHz Steinbrecher receiver.

Once the signal detection system detects a signal of interest, it will flag the drop receivers. For reasons of cost, the signal isolation function will be implemented using analog drop receivers (WJ-8617B) in Phase 2A. The narrowband output of these receivers will be digitized for processing by the VME-C30's in the ASPT. This will result in a loss of data equal to the latency delay of the signal detection processor.

In Phase 2B, shown in Figure 5.4, the isolation function will be implemented using digital filters and digital delay lines to compensate for the latency delay of the detection system [5]. These digital channel recovery processors will mix the signal of interest to near baseband, filter and decimate it for processing on C30's. The mixing will be done digitally and the filters will be linear phase FIR.

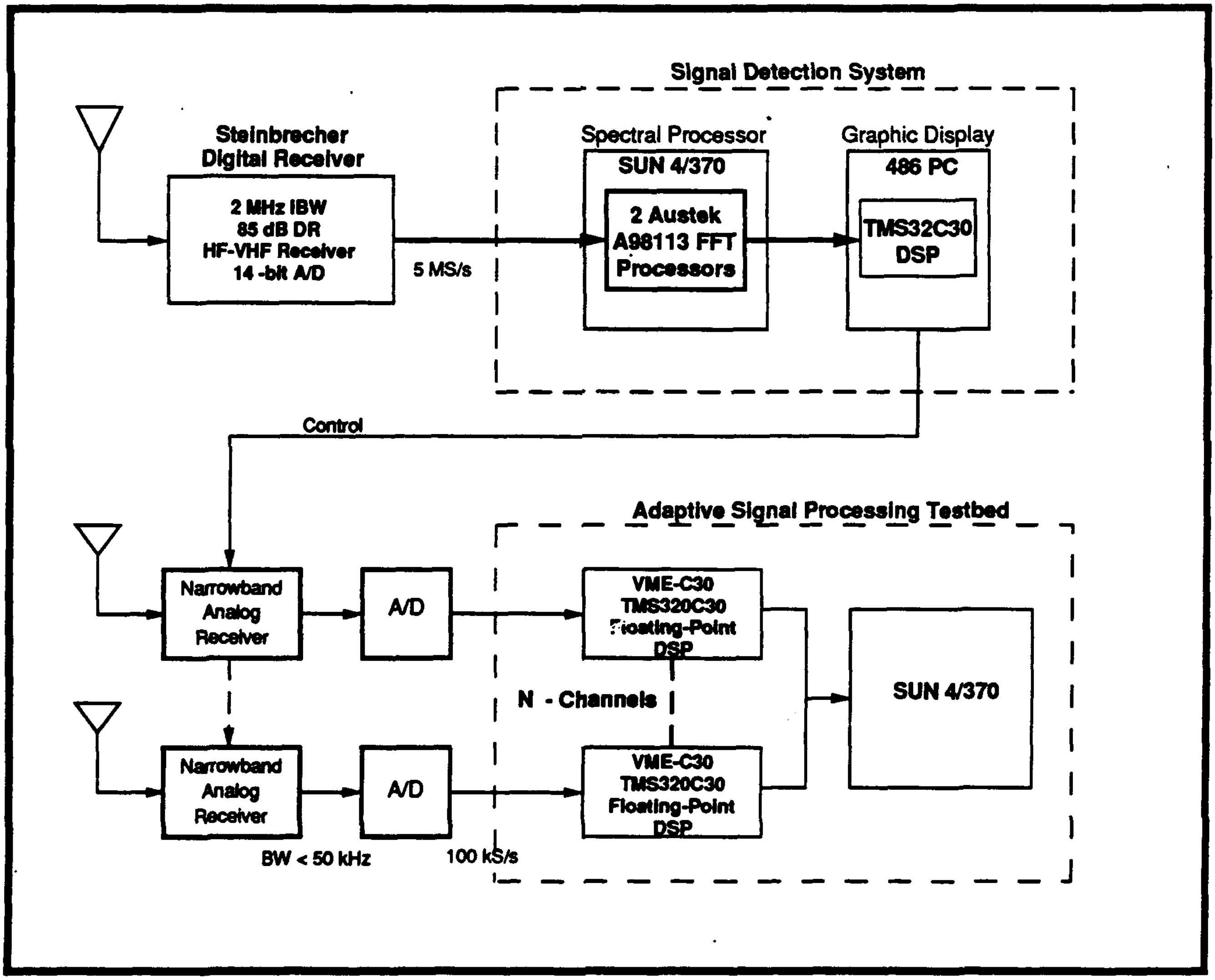

FIGURE 5.3: ACES PHASE 2A

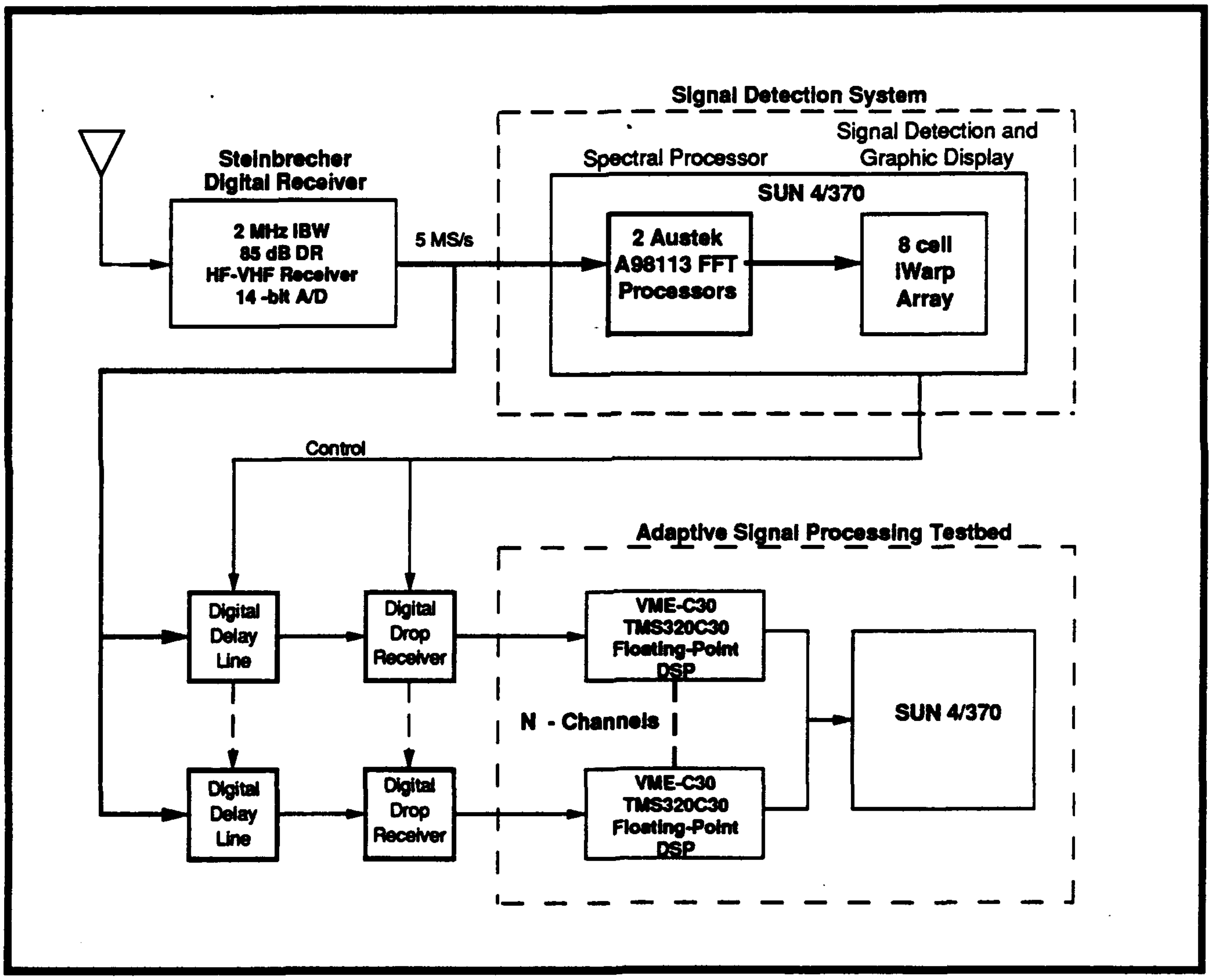

FIGURE 5.4: ACES PHASE 2B

5.2.6 **Digital Delay Lines**

The purpose of the digital delay line is to delay the data stream from the receivers to compensate for processing latency and phase delays. This component will be implemented using hardware First-In-First-Out (FIFO's). Three FIFO boards will be required for the three channel system. The risk is expected to be fairly low, although the boards will be a custom design.

5.3 **Phase 3**

This phase will address, in depth, the problem of DF'ing conventional and exotic emitters using various radio direction finding techniques. It will incorporate multiple wideband receivers to perform DF of low probability of intercept (LPI) signals. Increased processing capability, involving more iWarps or neural network devices, may be added to the testbed. Phase 2B will be used to determine what form and what level of processing will be required. This iterative approach is required in developing a system of this complexity. It is difficult to forecast at this point the exact system requirements. One possible system configuration is shown in Figure 5.5.

Another important part of this phase will be integration with the DFACTT to provide data fusion, EW analysis, and C^3I system functions. Once this is completed ACES will become a complete ESM system suitable for field trials.

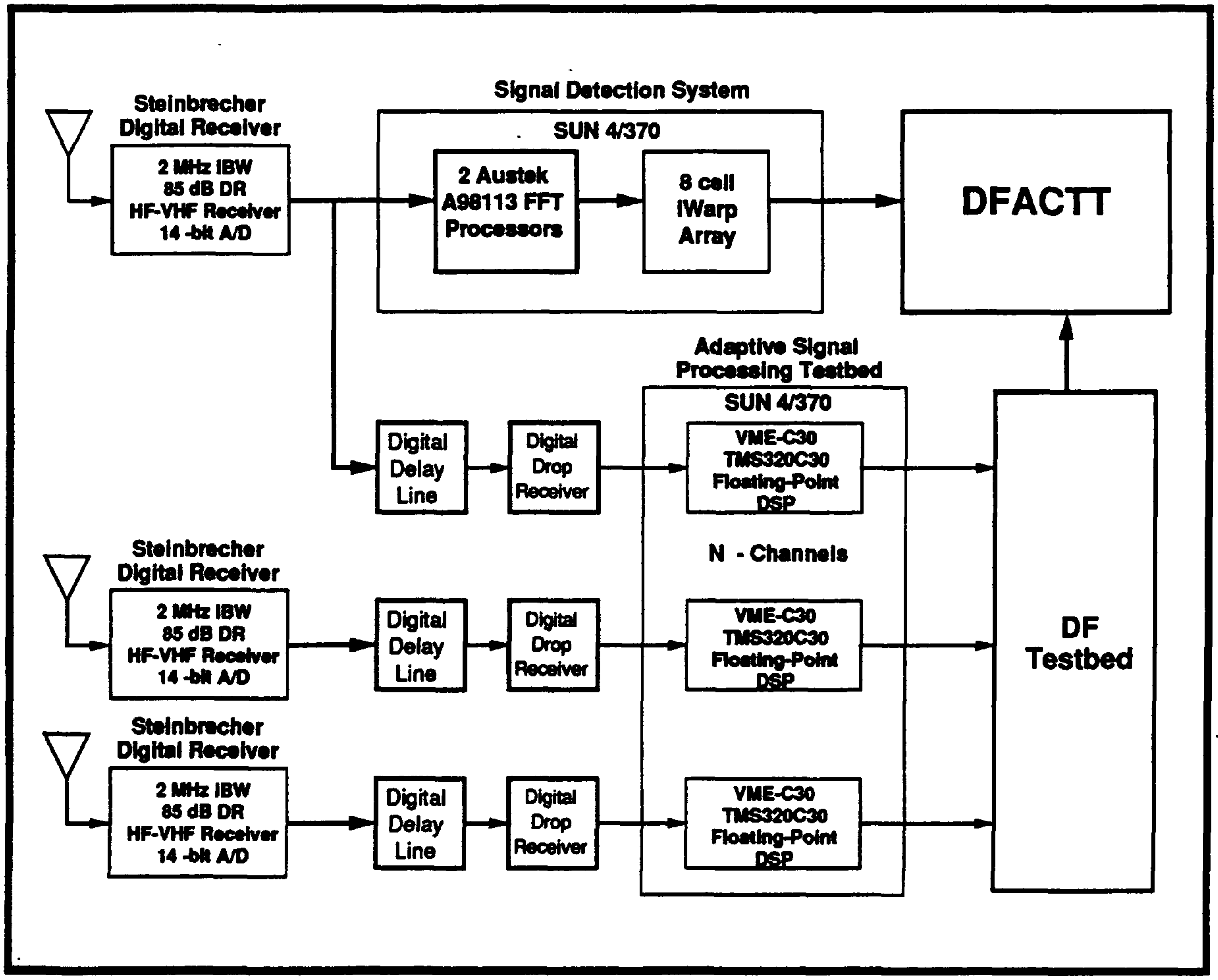

FIGURE 5.5: ACES PHASE 3

6.0 CONCLUDING REMARKS

The development of the Advanced Communications ESM System will be a significant challenge because of the use of state-of-the-art technologies in digital hardware, some of which are still experimental (e.g., iWarp array processors and neural networks); a fairly significant learning curve is anticipated for these areas. Other hardware components have only recently been incorporated into systems (e.g., the Austek FFT processors and C30 processor boards of the ASPT). For these technologies, however, a base of expertise already exists, which can be drawn on when required. Because of the requirement to have a flexible system to meet the ever challenging signal environment, the system will be completely programmable and will have advanced software tools to allow easy development of new algorithms. An important part of the project will be the integration and control of the various elements into a working system. The major reason for developing ACES over several phases is so that the expertise of DREO personnel and Canadian industry can be developed and utilized.

7.0 GLOSSARY

ACES	Advanced Communications ESM System
A/D	Analog-to-Digital Converter
AM	Amplitude Modulation
ASPT	Adaptive Signal Processing Testbed
BPSK	Binary Phase Shift Keyed
BW	Bandwidth
C^3I	Communications, Command, Control and Intelligence
DF	Direction Finding
DFACTT	Data Fusion and Correlation Techniques Testbed
DR	Dynamic Range
DS	Direct Sequence
DSP	Digital Signal Processor
ECM	Electronic Counter Measures
ESM	Electronic Support Measures
EW	Electronic Warfare
FFT	Fast Fourier Transform
FH	Frequency Hopping
FIFO	First-In-First-Out
FIR	Finite Impulse Response
FM	Frequency Modulation
FSK	Frequency Shift Keyed
HF	High Frequency (3 -30 MHz)
IBW	Instantaneous Bandwidth
IF	Intermediate Frequency
GFLOPS	Giga Floating Point Operations Per Second
LPI	Low Probability of Intercept
MFLOPS	Mega Floating Point Operations Per Second
MIPS	Mega Instructions Per Second
POD	Probability of Detection
POI	Probability of Intercept
QPSK	Quadri Phase Shift Keyed
SSB	Single Sideband
TH	Time Hopping
UHF	Ultra High Frequency (300 - 3000 MHz)
VHF	Very High Frequency (30 - 300 MHz)
VME	Virtual Memory Extension

8.0 REFERENCES

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[5] "An Analysis of Complex Down Mixing, Filtering and Decimation in ACES", Eric April, DREO Technical Note 91-2.

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